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| Cases | FS | Operation | F |
| A | 00101 | A - B | 11111111111111111111111111111100 (-4) |
| B | 01110 | NOT A | 11111110101010110010111010101111 (-22335824) |
| C | 00100 | A + 1’s c B | 11111111111111111111111111111011 (-5) |
| D | 00111 | A (00111) | 00000001010101001101000101010000 (22335824) |
| E | 00011 | A+B+1 | 00000010101010011010001010100101 (44671653) |
| F | 10100 | srB | 00000000101010100110100010101010 (11167914) |
| G | 00010 | A+B | 00000010101010011010001010100100 (44671652) |
| H | 11000 | slB | 00000010101010011010001010101000 (44671656) |
| I | 00000 | A (00000) | 00000001010101001101000101010000 (22335824) |
| J | 10000 | B | 00000001010101001101000101010100 (22335828) |
| K | 00001 | A + 1 | 00000001010101001101000101010001 (22335825) |
| L | 01100 | A XOR B | 00000000000000000000000000000100 (4) |
| M | 01010 | A OR B | 00000001010101001101000101010100 (22335828) |
| N | 00110 | A – 1 | 00000001010101001101000101001111 (22335823) |
| O | 01000 | A AND B | 00000001010101001101000101010000 (22335824) |

The functional unit takes in two 32-bit values and performs various operations on them based on the value of the 5-bit FS signal. In this case, A was 00000001010101001101000101010000 (22335824) and B was 00000001010101001101000101010100 (22335828). These functions are performed through instantiations of the Arithmetic Logic Unit and the Shifter, as seen in the schematic, with these values being outputted based on a 2 to 32 bit multiplexer.